

METROLOGY AND MEASUREMENT SYSTEMS

Index 330930, ISSN 0860-8229 www.metrology.wat.edu.pl



# THE IMPACT OF DIGITAL DELAY LINES' SPATIAL ALLOCATION ON THE DPS SYNCHRONIZATION QUALITY

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#### Abstract

The paper concerns the optimization methodology of design of a high-resolution digital phase synchronizer (DPS) module cooperating with a multi-channel coincidence counter. The main function of the DPS module was to guarantee a high synchronization between the measurement system and trigger pulses (with various repetition rates) from the photo detector. With this approach, it became possible to adapt the measurement system to work with a wide spectrum of excitation sources while maintaining the required metrological parameters. The DPS resolution is determined by the architecture of coding tapped delay lines (TDLs) utilized, whereas the synchronization degree by the differences in their integral nonlinearity errors ( $\Delta R_{INL}$ ). In traditional DPS designs, the basis for synchronization were single TDLs built on arithmetic carry chain paths, which are usually characterized by high nonlinearity. The approach presented in this paper assumes the use of complex tapped delay lines (CTDLs) and appropriate selection of spatial TDLs allocations within a programmable logic structure. The proposed solution enables effective minimization (from 62.6 ps to 26.2 ps) of the synchronization error between the measurement system and the investigated process.

Keywords: Programmable logic structures, Delay lines, Phase synchronizer, Time interval measurement.

## **1. Introduction**

The field programmable gate arrays (FPGAs) structures, alongside application-specific integrated circuits (ASICs), remain a popular choice for time to digital converters (TDCs) implementations [1-9]. The main factors that decide about this are the shorter development time and lower costs than in ASICs, as well as the possibility of reprogramming. An undesirable feature of FPGA-based prototyping is variation in time bin sizes of *tapped delay lines* (TDLs), which leads to nonuniformity and degradation of the TDC time resolution. To improve nonlinearity and reduce bin size, the method of comparing time bins from multiple TDLs is usually used [10-14]. Unfortunately, the complex tapped delay lines (CTDLs) architecture needs greater resource requirements and can be difficult to implement in small FPGA structures. The recommended solution in this situation may be increasing the time standard frequency and applying a line selection algorithm [15]. The digital phase synchronizer (DPS) resolution is determined by the architecture of TDLs, but the quality of synchronization degree, by  $\Delta R_{INL}$ errors. In traditional DPS designs [16], the principle of synchronization was implemented based on single TDLs, which were characterized by relatively high nonlinearities. The use of multiple delay lines and appropriate selection of TDLs spatial allocations [17-18] within FPGA devices allows for improving the quality of DPS synchronization. This article provides crucial information on the multi-segment digital TDL allocation process used to create CTDL, preferred to obtain greater time resolution and linearity of the DPS module. The obtained results

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confirm the validity of the adopted assumptions and the effectiveness of optimizing the DPS implementation process, specifically in terms of increasing its resolution, without having the needs to change the applied technology.

This article is organized as follows. In Section 2, a simplified block diagram and main information of DPS functionality are presented. The AMD FPGAs series SLICE architecture and global clock network are described in Section 3. This chapter also provides information on the design of multiple delay lines and potential places of their allocation in the FPGA structure. At the end, it was explained the TDL's segment sorting methods used for bubble errors minimization. In the next section, we included the experimental tests results, obtained for four most favourable implementation groups. In each group, a delay line selection algorithm has been applied to obtain the optimal implementation of CTDL. In this chapter, the test results, compared to the plain allocation and tuned TDLs implementations, are also describes in details. Finally, we presented the segment mapping procedure preferred for the highest quality of DPS synchronization. Finding the optimal CTDL implementation is the main goal of this work.

#### 2. DPS architecture

The simplified block diagram of the DPS module is presented in Fig. 1. The basic functional elements of the DPS module are high-resolution TDLs. Such TDLs are the main components for the development of two important DPS sub-modules, namely: the *phase detection module* (PDM) and the *delay selection module* (DSM). The DPS architecture presented in [16] involves the use of two TDLs, one in each of DPS sub-modules. The approach proposed in this article is based on the CTDL architecture and assumes selecting four TDLs in PDM and two TDLs in DSM modules. The PDM and DSM modules are responsible for precise phase detection of reference clock signal and ensuring effective synchronization among synchronized signals.



Fig. 1. Simplified block diagram of the DPS module.

Information about the time relation between the main clock and the trigger pulse is represented at the PDM outputs in a pseudo-thermometric code. Based on this code, the correct mapping procedure in the DSM module is executed using a switching matrix. The required number of TDL segments in both modules is determined by the period of clock signal, which is the time base of the measurement system. In the case under consideration the DPS module

Metrol. Meas. Syst., Vol. 32 (2025), No. 3 DOI: DOI: 10.24425/mms.2025.154677

was clocked with a reference clock signal of 350 MHz, obtained from digital frequency synthesis process. The built-in FPGA structure, the *Digital Clock Manager* (DCM) blocks were used for this purpose. The TDLs resolutions for two flip-flops architecture (placed in SLICE) were approximately 22.5 ps. This implied the use of a TDL line consisting of at least 127 delay segments, respectively. The implementation of CTDL lines increases the number of active delay segments used to build PDM and DSM. Required logical resources typically grow proportionally to the number of TDLs used for CTDL creation.

## 3. Multiple TDLs implementations

*Configurable logic blocks* (CLBs) are basic logic resources intended for implementing sequential and combinational circuits in FPGAs. Each CLB block contains four SLICE cells, grouped in two pairs and built-in separate columns of the FPGA (Fig. 2). SLICEs are routed individually by independent carry chain paths dedicated to implement arithmetic functions. The chip columns (marked by the manufacturer with X symbols) are grouped by eight with respect to the areas reserved for the implementation of memory and multiplication blocks.



Fig. 2. FPGA device architecture: the skew diagram of clock signal distribution in the GR1 allocation area for selected columns X0 (a) and X7 (b), and then within the GR2, GR3, GR4 allocation areas (c); device topology, potential TDL allocation groups, and logic resources construction (d).

The global clock lines designed to support high frequency signals are spreading from the central part of the chip. To achieve uniform even signal distribution and ensure comparable timing parameters across the chip, a mechanism of to divide the structure into clock regions was used. The signal distribution delays obtained within a single clock region and between clock regions (for the GR1-GR4 groups) are shown in Fig. 2a-c. The signals skew inside the clock regions are comparable and do not exceed more than 25 ps, while between neighbouring segments it is only 5 ps. A completely different situation occurs at the border of clock regions. In this case, the signal skew increases dramatically, reaching 32 ps.

The proposed FPGA architecture allows the implementation of 32 independent TDLs with 256 taps placed inside the 32 CLBs. Each of TDLs were built from carry chains components, such as MUXCY, XORCY, FDCE, used for forming fast arithmetic transfers. The non-standard use of these components, the technological spread of the used resources and also the differences in signal propagation times have a significant impact on the high non-linearity of the transfer characteristics of TDLs, which can lead to bubble errors [19] at the processing stage (Fig. 3b).



Fig. 3. The multiple delay line creation (a) [10] and segments sorting procedure (b) [15] used for the bubble errors minimization.

Bubble errors may be responsible for the malfunction of the phase decoder, which may return incorrect values during the conversion process [20-21]. The use of proper TDL segment sorting methods (Fig. 3b) minimizes bubble errors and ensures the correct operation of the DPS module. The procedure for creating CTDL lines (Fig. 3a) requires the determination of the transfer characteristics of the TDLs and the relative shifts  $\Delta t_{di}$  between the lines. This procedure is described in detail in [10].

#### 4. Experimental results

Experimental tests, performed to identify the timing parameters of the implemented lines, were carried out using the ML403 hardware platform. In the area of all possible DPS allocations, four most favourable implementation groups (GR1-GR4) were identified. Within

each of groups, eight TDL lines were implemented in the appropriate columns of the FPGA device. The XC4VFX12 FPGA device architecture allows TDLs implementation with  $q_{eqv}$  resolutions [10] ranging from 26.76 ps to 30.87 ps. Transfer characteristics for three randomly selected TDLs are shown in Fig. 4.



Fig. 4. TDL characteristics for GR1, GR2 and GR4 allocation areas.

As illustrated in Fig. 4, the TDLs implemented in GR1 and GR2 groups show worse timing parameters (less uniformity of bin widths) than those in GR4. This comes from the fact, that the GREG1-GREG2, GREG2-GREG3 and GREG5-GREG6 nonuniformities between clock regions (Fig. 2a-c) do not expanded across the GR4 group. Due to the above feature, typical for the FPGA technology, it was necessary to identify the correctness of the TDL processing. For this purpose, using the code density test method [22], a series of TDL experimental tests were performed. Each time, the states of the FDCE outputs (flip-flops in SLICEs) were recorded directly, bypassing the code converters. Unfortunately, when analyzing the test results, bubble errors were detected during the conversion process. For this reason, an appropriate sorting procedure was carried out according to the scheme shown in Fig. 3b. Finally, the correct orders of the delay segments were established. The results of the  $q_{eqv}$  resolution for the individual TDL allocation areas are summarised in Table 1.

The best performance of TDL allocations was obtained for the GR4 area. For this allocation, no significant deviations in the global clock distribution network delays at the clock domain boundaries are observed. The evaluated average  $q_{eqv}$  resolution value of the TDLs was 27.73 ps, while the averaged maximum of *integral nonlinearity error* (INL) equals 1.7 ps. The TDLs in GR1, GR2 and GR3 areas were characterized by worse results. Their average  $q_{eqv}$  resolutions were 28.44 ps, 28.94 ps and 28.74 ps.

The final step in the CTDL formation procedure was to determine the propagation times of the routing signals entering the TDLs. The measurement was carried out for each of the four allocation areas. The results for selected GR3 and GR4 groups are shown in Table 2.

GR 1	X0	X1	X2	X3	X4	X5	X6	X7
	29.75 ps	28.27 ps	28.71 ps	28.27 ps	28.92 ps	27.88 ps	27.99 ps	27.74 ps
GR 2	X24	X25	X26	X27	X28	X29	X30	X31
	30.04 ps	28.84 ps	28.77 ps	28.14 ps	28.79 ps	29.76 ps	28.73 ps	28.45 ps
GR 3	X32	X33	X34	X35	X36	X37	X38	X39
	30.87 ps	28.52 ps	28.57 ps	28.95 ps	28.13 ps	28.06 ps	27.45 ps	29.36 ps
GR 4	X40	X41	X42	X43	X44	X45	X46	X47
	26.76 ps	28.01 ps	29.30 ps	28.06 ps	28.14 ps	27.37 ps	27.03 ps	27.18 ps

Table 1. The  $q_{eqv}$  resolutions of the TDLs implemented in eight possible locations.

Table 2. Propagation times  $\Delta t_{di}$  of paths for two randomly selected groups.

23	X32	X33	X34	X35	X36	X37	X38	X39
61	24.28 ps	20.11 ps	5.49 ps	20.93 ps	7.60 ps	0 ps	32.39 ps	35.03 ps
GR 4	X40	X41	X42	X43	X44	X45	X46	X47
	11.01 ps	1.56 ps	13.42 ps	3.09 ps	0 ps	15.72 ps	21.75 ps	22.78 ps

The maximum spreads of propagation times  $\Delta t_{di}$  obtained for individual groups from GR1 to GR4 were 28.11 ps, 32.26 ps, 35.03 ps and 22.78 ps, respectively. The above scatters have a significant impact on the process of assembling the CTDL lines. As a result of the assembly of TDLs with similar characteristics, *e.g.* with dominant wide bins at the region boundaries, further accumulation of bins with larger widths is observed (Fig. 5).



Fig. 5. Bin widths of CTDL4 and CTDL2 placed in GR1 allocation area.

Of course, the above situation is not always guaranteed. The bin widths, in the best-case scenario, may be divided, while in the worst-case, they may accumulate. The first situation may occur when multiple narrow bins from one TDL line are assigned to a wide bin in another line.

As a result, such a bin ceases to be dominant in the CTDL characteristics. On the other hand, partial coverage of dominant bins increases the probability of the accumulation of areas with dominant bins widths. For this reason, it is crucial to select appropriate TDLs by examining all possible configurations.

Achieving a higher resolution of CTDL requires combining of more TDLs. This would be easiest to obtain for eight TDLs in a group, due to the single folding of all TDLs (Fig. 6).

The situation is more complicated for a smaller number of TDLs (from the set of eight TDLs), where the number of possible line combinations increases. The number of different combinations of four TDLs from an eight-element set is 70. Whereas for two TDLs from four possible areas it is smaller and amounts only 6. For this reason, 76 combinations of TDL compositions were analyzed for each of the four allocation areas (GR1-GR4).

The conducted research allowed the identification of relationships describing the impact of selecting a specific spatial configuration of TDLs on the parameters of newly created CTDLs. Applied for this purpose, the line selection algorithm, directly checked of all possible TDL combinations [15]. Based on this, the equivalent resolution limits of the CTDLs used in the implementation of DPS module were determined. The results are shown in Fig. 7a.

In the graph, the  $q_{eqv}$  resolution results of the CTDL lines (obtained for the GR4 group) are indicated in black. Moreover, the comparative result of implementing a single TDL with  $q_{eqv}$  of 13.26 ps in the Kintex UltraScale XCKU040 device is also plotted there (dashed line). To obtain consistent results, the selection of four TDLs in group GR4 is sufficient, but the use of three TDLs may be not guaranteed (Fig. 7a).

The best TDL configurations and the parameters of the newly created CTDLs for the specified allocation areas are summarised in Table 3.



Fig. 7. The CTDL equivalent resolution  $q_{eqv}$  vs the number of TDLs involved (a) and the results of segment mapping in PDM and DSM sub-modules (b).

Allocation area	The best configuration in the PDM module	The best configuration in the DSM module	Equivalent resolution for CTDL in PDM	Equivalent resolution for CTDL in DSM
Group 1	[X3, X4, X6, X7]	[X1, X2]	9.75 ps	16.78 ps
Group 2	[X25, X27, X29, X30]	[X24, X31]	9.97 ps	17.69 ps
Group 3	[X32, X35, X36, X37]	[X34, X39]	9.42 ps	16.66 ps
Group 4	[X40, X41, X46, X47]	[X43, X45]	9.45 ps	15.65 ps

Table 3. The best TDL configurations and CTDLs timing parameters.

Example characteristics of CTDL4 and CTDL2 obtained for the most favourable TDLs implemented in the GR2 allocation area are shown in Fig. 8.



Fig. 8. Bin widths of CTDL4 and CTDL2 placed in GR2 allocation area.

The probability of the accumulation of areas with dominant bins widths observed in Fig 8 remains still noticeable, but not as significant as in Fig. 5. The implementation of four and two TDLs in the PDM and DSM modules allowed achieving resolutions of 9.97 ps and 17.69 ps, respectively. The best composition of four *TDLs* (CTDL4) yields 511 delay segments, but a composition of two TDLs (CTDL2) yields only 254. This situation is consistent with the fact that for CTDL transfer characteristics with predominantly larger bin widths, a smaller number of delay segments is required to cover the same range. This is particularly evident when the transfer characteristics are highly non-linear.

The further optimisation process concerned the selection of allocation within GR4 group with the most favourable timing parameters. By implementing the TDLs within the area indicated in Fig. 4 (red dashed line), the average  $q_{eqv}$  resolution value of 24.58 ps was obtained. The CTDL4 line built at this location had approximately 543 delay segments. The difference in the number of required segments was mainly caused by the extra wide bins in the initial line segments (GREG4), which had to be split into more segments with shorter times in the target allocation. Example characteristics of CTDL4 and CTDL2 obtained for TDLs implemented in the GR4 MFA allocation area are shown in Fig. 9.

The best  $q_{eqv}$  resolution results of the CTDL lines obtained for the GR4 MFA group after omitting the first 64 line segments are also indicated in Fig. 7a (red line). To obtain consistent

results to Kintex UltraScale structure, the use of three TDLs would be required, while the selection of four TDLs makes it possible to achieve resolutions of 9.4 ps.

The cross-mapping of CTDL line segments in the PDM and DSM is the basis for synchronisation of the DPS module (Fig. 7b). This procedure involves assigning PDM to DSM segments for which the delay mismatch errors will be the smallest. The highest degree of synchronisation is achievable for ideal TDLs with the same resolution. For real TDLs, it is necessary to identify the INL errors of both modules. The differences in INL errors are responsible for the precision of the time interval mapping by the DSM module. For experimental purposes, in the first approach, measurements were performed for single TDL lines. The determined differences of integral nonlinearity errors  $\Delta R_{INL}$  (for a two flip-flops architecture) did not exceed 23.1 ps. The associated maximum range of all non-linearity values reached about 36.5 ps in this case.



Fig. 9. Bin widths of CTDL4 and CTDL2 placed in GR4 MFA allocation area.

The test results for the best CTDL configuration are shown in Fig. 10a. The maximum value of the difference between TDLs linearity errors in this case was 8.6 ps. The obtained maximum range of determined  $\Delta R_{INL}$  differences was 16.7 ps, whereas its average value was equal to 2.85 ps. By limiting the mapping to the most favourable routings only, the above  $\Delta R_{INL}$  values were compensated to approximately 6.2 ps. The maximum range of all non-linearity values and mean values were 12.1 ps and 1.65 ps, respectively. The result of the final compensation is shown in Fig. 10b.



Fig. 10. Synchronization results for all (a) and most favourable (b) routings.

#### 5. Conclusions

As shown in this paper, the use of the TDLs selection algorithm allows to obtain better  $q_{eqv}$ resolution without incrementing the required hardware resources. Determined relations between the  $q_{eqv}$  and the number of TDLs allow to estimate the upper limit of resolution that can be achieved for given FPGA chip. The implementation of eight TDLs allows to achieve a resolution of 5.74 ps, which is an improvement of 7.56 ps compared to the implementation of a single TDL in the Kintex UltraScale device. This research provides an opportunity to restore the oldest solutions to parameters comparable to implementations in newer FPGA structures. In this way, the DPS module optimization process allowed for the improvement of synchronization by almost seven times better compared to the ordinary implementations. This was done at the cost of additional logical resources, necessary to build the CTDL line. Importantly, randomly combined TDLs only sporadically improve the CTDLs performance. Therefore, the random TDLs configuration providing similar parameters to the Kintex UltraScale TDLs, required the use of three TDLs implemented in the MFA area (Fig. 7a). Implementation outside this area requires the use of four TDLs configured randomly. Using the best TDL configurations (chosen according to the line selection algorithm) allows to reduce the required number of TDLs to three, regardless of whether they are implemented in the MFA area. The above number of TDLs is acceptable for implementations in small FPGA structures.

The ranges of  $q_{eqv}$  achievable with a fixed number of TDLs is particularly important from the perspective of developing the DPS module. The TDL selection method used in this paper identified the potentially best allocation for placing a DPS module in the programmable structure. The tests were performed for XC4VFX12 device. Four areas of possible DPS module allocations were investigated. Choosing the right spatial allocation and the use of multiple lines in the selected region allowed to at least a 70% improvement of  $q_{eqv}$  resolution and ensured effective minimization of  $\Delta R_{INL}$  differences from 23.1 ps to 6.2 ps. This reduced the synchronization error of the DPS module from 62.6 ps up to 26.2 ps.

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