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HIGH TIMING RESOLUTION PULSE WAVEFORM SYNTHESIS BASED ON FEATURE-FITTING

Yujie Deng, Zaiming Fu, Hanglin Liu, Dexuan Kong, Xin Ai

University of Electronic Science and Technology of China, School of Automation Engineering, Chengdu 611731, China
(✉ *fuzaimin@163.com,+86 61831321*)

Abstract

With the widespread demand for high-precision controllable pulse signals in electronic systems such as communications, radar, and quantum computing, the timing resolution and waveform flexibility adjustment capability of excitation signal sources are more demanding. However, *direct digital synthesis* (DDS) techniques are limited by timing resolution, while computational synthesis methods are computationally complex and resource-consuming despite higher accuracy. In this paper, an improved DDS pulse waveform synthesis method is proposed, which effectively reduces the storage requirement by storing only the pulse waveform edge samples as feature samples instead of all the samples in the complete waveform period. Meanwhile, combining with the adaptive phase adjustment algorithm, the phase offset value is calculated based on the overflow result of the phase accumulator, and the edge position is adjusted to realize the waveform fitting with higher timing resolution. The feature-fitting scheme streamlines the data storage content while avoiding the complexity of real-time computation, achieving a balance between computational resources and memory usage. The method uses 1 GSPS sampling rate and 1 BRAM to successfully synthesize pulse waveforms with timing resolutions of 100 ps and 10 ps, realizes edge time and amplitude adjustments, and achieves a rms jitter of 10.04 ps. The method provides a feasible solution for high-precision pulse signal synthesis with low storage occupation, and provides theoretical and practical support for the realization of high-performance electronic test equipment..

Keywords: waveform synthesis, feature-fitting, high resolution, DDS.

1. Introduction

High-precision, controllable pulse signals play a crucial role in the research and testing of electronic systems [1–5]. In communication systems, impulse excitation is a common method for measuring the impulse response of communication channel, particularly in wireless communications, where it is used to analyze and compensate for multipath and fading effects [6–8]. Impulse excitation is the fundamental technology underlying *ultra-wideband* (UWB) communication systems, which utilize narrow pulses to transmit information [9–11]. Furthermore, pulse excitation is a prevalent technique in radar and imaging systems. Pulse radar determines information such as the distance and speed of a target by transmitting a pulse signal and detecting the time and intensity of the reflected pulse [12–14]. In quantum computing systems, high-precision pulse excitation is used to accurately initialize, control, and measure quantum bits [15,16]. With the rapid development of nanotechnology, its role in realizing high-density memories, faster processors, and low-power electronic devices, especially in the semiconductor field, has become increasingly important. Researchers need to fully characterize the properties of devices and materials using small amplitude signals and repeatable measurements [17,18]. Currently, there is an increasing demand for pulse waveform synthesis with high-resolution timing characteristics and precise and controllable pulse waveforms in

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various fields. Moreover, the demands for timing resolution, accuracy, and jitter performance of pulse signals are also increasing [19].

The conventional method for generating pulse signal relies on analogue typically using an oscillation loop to generate the pulse waveform [20]. However, the pulse waveform generated by the oscillating circuit has a limited range of adjustable parameters, making precise quantitative adjustment challenging. As digital technology continues to evolve and become increasingly sophisticated, digital circuits are gradually replacing traditional analogue circuits in the pulse signal generation. The application of digital pulse synthesis technology reduces the size of the pulse signal synthesis circuit, while also extending the frequency coverage and output level range. Moreover, digital circuits significantly enhance the programmability of pulse signals. The current methods for generating pulses based on digital circuits include: pulse generation by counter, pulse generation by relative delay technique combined with D flip-flop, and so on [21–23]. Despite the advantages of digital pulse synthesis technology, precise control of the pulse amplitude, rise time and fall time is still not fully achievable without the assistance of additional circuits.

Direct Digital Synthesis (DDS) is one of the most widely used waveform synthesis techniques. The basic block diagram of pulse waveform synthesis based on DDS technique is shown in Fig. 1, which includes modules such as the phase accumulator, waveform memory, *digital-to-analog converter* (DAC), low-pass filter and clock generator [24]. The *N-bit* phase accumulator accumulates with the frequency control word *K* under a fixed sampling clock and accesses the waveform memory by using the top *M bits* of the accumulation result as the memory address. The waveform memory outputs the digital amplitude information of the pulse waveform, which is subsequently converted to an analog waveform by a DAC. The advantage of DDS pulse waveform synthesis is that it enables precise and rapid control of the frequency, phase, and amplitude of the synthesized waveform in digital signal processing [25–27]. However, the achievable timing resolution is inherently limited by the time interval between sampling points. To mitigate this limitation in synthesizing pulse parameters, it is possible to accurately calculate the voltage value of each sample point in each clock cycle by means of pulse parameter calculations [28–30], enabling precise control of parameters such as pulse width, rise time, fall time and pulse delay.

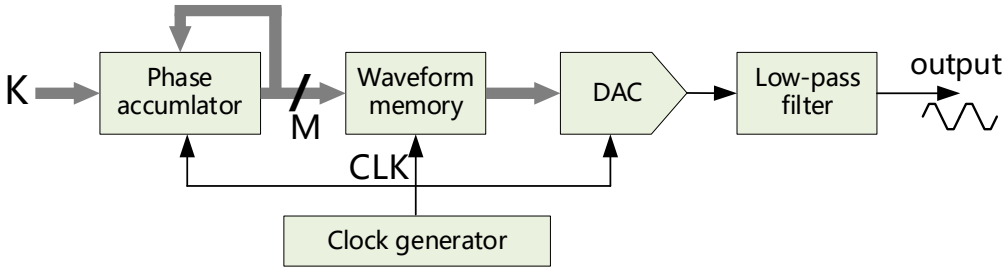

Fig. 1. DDS architecture.

We propose a feature-fitting scheme based on DDS, where the principle of feature-fitting pulse waveform synthesis stores the pulse edges as features to fit the correct pulse waveform. The waveform memory in the DDS, which previously stored samples for an entire waveform period, is now modified to store only the pulse edge samples. And an adaptive phase adjustment algorithm will be added, this algorithm can calculate the edge offset position just based on the phase overflow value of the phase accumulator. Thus, it is able to adjust the positions of the rising and falling edges independently and accurately to achieve high timing resolution. The main contributions of this method are:

1) By adopting the feature mapping memory method, it solves the problem that the ordinary DDS scheme leads to the distortion of the timing characteristics of pulse edges under the limitation of memory capacity, and improves the pulse resolution.
2) An adaptive phase adjustment algorithm is proposed to address the challenge of calculating sample points of mapped edge waveforms, thereby reducing the need for extensive pre-processing steps and computational resources.
3) To validate our approach, we implemented pulse synthesis pulse synthesis with a 100 ps and 10 ps on a Xilinx FPGA XCKU040, paired with a DAC39J82. The results demonstrate that this method not only achieves high-resolution pulse waveform synthesis, but also effectively conserves resources.

2. Architecture and principle

2.1. Edge adjustment principle

The pulse waveform is primarily divided into four parts in the time domain: rising edge, high-level, falling edge and low-level. In the high-level and low-level regions, the waveform sample points are constant values and do not contain meaningful information about level transitions. To accurately reconstruct the pulse waveform in the time domain, it is sufficient to precisely describe only the rising and falling edges. Based on this characteristic, we modify the waveform samples stored in the DDS waveform memory for the entire cycle to store only the feature samples, *i.e.*, edge waveform samples, that represent the entire pulse waveform. The key to achieving high timing resolution is the ability to precisely adjust the position of the rising and falling edges, the principle of which is shown in Fig. 2.

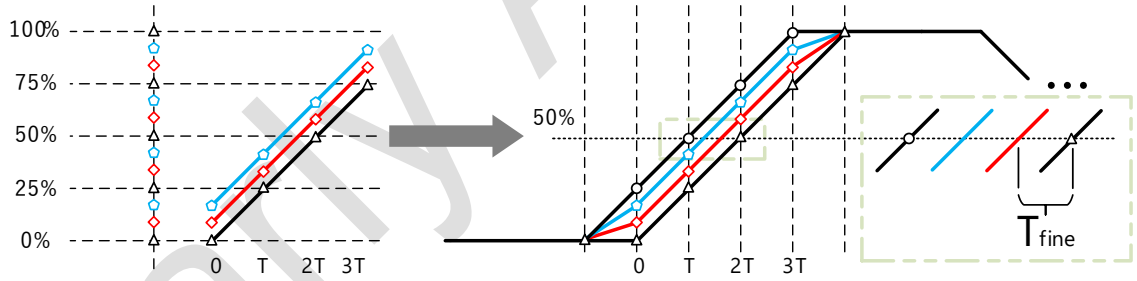

Fig. 2. Edge adjustment.

The black triangular sample points in Fig. 2 represent the initial edge sample points, with the edge consisting of four sample points. The neighboring black triangle waveform samples are divided into three equal amplitude parts to obtain the red rhombic and blue pentagonal samples, respectively. In the time domain, the red rhombic sample points and blue pentagonal sample points are mapped as pulse edges. It can be observed that the edges formed by connecting the black triangular sample points gradually shift upwards, transitioning into the red and blue edges. When these red and blue edges are incorporated into the pulse waveform. The edge is effectively shifted left by T_{fine} or 2 T_{fine} relative to the time axis, with minimal change in edge timing. A sample clock period T is divided into three parts by T_{fine} equalization, which means that three equal divisions of the adjacent samples in amplitude can improve the time resolution by a factor of three. As the number of equal amplitude fractions of adjacent waveform samples increases, so does the time resolution that can be achieved.

To illustrate the edge change process more concretely, we set the DAC's waveform sampling rate f_S to 1 GSPS (with a sampling period T_S of 1 ns) and the vertical resolution N_{DAC} to 12 bits.

The edge time of the pulse T_{edge} is 3.2 ns and the timing resolution to be achieved is T_{res} of 0.1 ns. This means that the timing resolution is improved by a factor of 10 compared to 1 ns, so the amplitude of two adjacent waveform samples is divided into 10 equal parts. According to the definition of pulse edge time, the edge of the whole 3.2 ns/0.8 ns = 4 ns, can be derived from (1) contains 4 sampling points, recorded as N_{edge}. And according to (2), the total number of edge samples must be stored for 4 × 10 = 40, recorded as N_{total}. With a vertical resolution of 12 bits, the digital waveform sample point value range is 0 to 2^{12}-1 (0 ~ 4095).

$$N_{edge} = \left\lfloor \frac{T_{edge}}{0.8 \times T_S} \right\rfloor \tag{1}$$

$$N_{total} = \left\lfloor \frac{T_S}{T_{res}} \times \frac{T_{edge}}{0.8 \times T_S} \right\rfloor = \left\lfloor \frac{T_{edge}}{0.8 \times T_{res}} \right\rfloor \tag{2}$$

The edge left shift time is T_{fine}, when T_{fine} is 0 ns, the values of the four sample points are 0, 1024, 2048 and 3072 respectively, and when T_{fine} is 0.1 ns, the values of the sample points *S1*, *S2*, *S3*, and *S4* are 102.4, 1126.4, 2150.6, and 3176.8 respectively. The sample point values are derived from (3), and the values of all edge waveform sample points are listed in Table 1.

$$Sn = \frac{T_{fine} \times 2^{N_{DAC}}}{T_{res} \times N_{total}} + \frac{n \times 2^{N_{DAC}} \times 0.8 \times T_S}{T_{edge}} \tag{3}$$

Table 1. Waveform sample point value.

T_{fine} (ns)	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
S1	0	102.4	204.8	307.2	409.6	512	614.4	716.8	819.2	921.6
S2	1024	1126.4	1228.8	1331.2	1433.6	1536	1638.4	1740.8	1843.2	1945.6
S3	2048	2150.4	2252.8	2355.2	2457.6	2560	2662.4	2764.8	2867.2	2969.6
S4	3072	3174.4	3276.8	3379.2	3481.6	3584	3686.4	3788.8	3891.2	3993.6

It can be seen that the adjacent waveform samples are divided into 10 equal parts, while all the edge waveform samples divide the vertical range of 4096 into 40 equal parts. The waveform sample points are stored sequentially from 0 to 3993.6, with the amplitude difference between adjacent sample points being 102.4. If the address of the sample points is 1, 2, 3, ..., 40, then the total memory capacity of the edge sample points is 40 × 12 bits = 480 bits. The values of the waveform sample points in the table include fractional parts, which are rounded down when stored, and only the integer parts are stored. Under the above conditions, the maximum error *e* caused by the fractional part is less than the error caused by changing the sample point value by 1. The theoretical time change caused by changing the sample point value by 1 is 1/4096 × 4 ns = 0.98 ps, so the error is less than 0.98 ps at an edge time of 4 ns. Since the timing resolution of the edge is not constrained by the edge time, the edge time is adjustable. *Equation* (4) shows the relationship between *e* and edge time. It can be concluded that the maximum error from the fractional part decreases as the edge time shortens.

$$e < \frac{T_{edge}}{2^{N_{DAC}}} \tag{4}$$

The required capacity *M* of the waveform memory depends on the timing resolution T_{res}, edge time T_{edge} and vertical resolution N_{DAC} to be implemented and is independent of the waveform sampling rate T_S. The memory capacity can be calculated using (6). The upper limit of the pulse timing resolution that can be achieved by this method without limiting the

waveform memory capacity is given by (5). *From* (6) it can be concluded that the memory capacity is still related to the edge time when the timing resolution and vertical resolution are determined. However, by analyzing the relationship between the edge time and the theoretical upper limit of the timing resolution, it can be seen that when the edge time reaches $2^{N_{DAC}} \times T_S$, the amplitude difference between adjacent waveform samples can no longer be distinguished. For this method, the maximum capacity of the waveform memory should be calculated according to (7). If the synthesis edge time exceeds $2^{N_{DAC}} \times T_S$, it can be achieved by adjusting the bit width of the edge address generator.

$$T_{res} = \frac{T_S}{2^{N_{DAC}}} \tag{5}$$

$$M = N_{total} \times N_{DAC} = \left\lfloor \frac{T_{edge}}{0.8 \times T_{res}} \right\rfloor \times N_{DAC} \tag{6}$$

$$M_{\max} = (2^{N_{DAC}} \times N_{DAC}) \tag{7}$$

2.2. Synthesis process

The principle of feature-fitting pulse waveform synthesis is shown in Fig. 3 and consists of a phase accumulator, waveform state selector, edge address generator, edge memory and DAC. The phase-to-address mapper consisting of the waveform state selector and the edge address generator is a new module added to the DDS structure and is responsible for generating the shifted edge address.

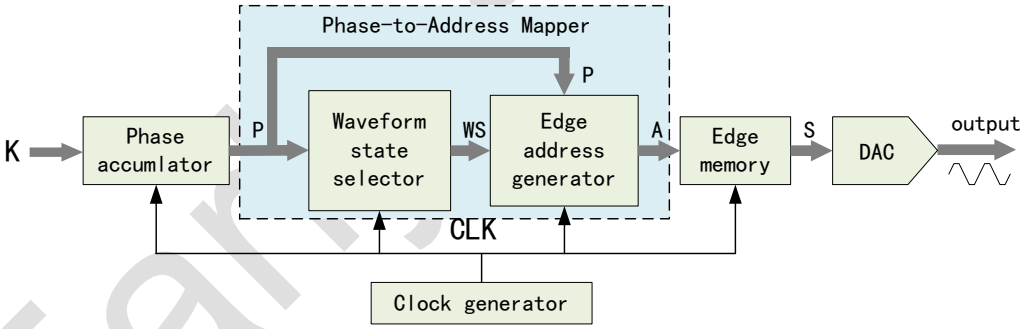

Fig. 3. Principle of pulse synthesis for feature-fitting.

The clock generator provides a reference clock for all modules. The phase accumulator calculates the pulse phase *P* based on the waveform frequency control word *K*. The waveform state selector determines the waveform state *WS* according to the phase value *P*. The edge address generator generates the corresponding address *A* based on the state flag *WS* and the phase value *P*. The edge memory stores the waveform edge sample points *S*. Finally, the DAC converts these sample points *S* into the desired pulse waveform.

The pulse waveform generation process is shown in the Fig. 4: when the phase value accumulates to the phase corresponding to the rising edge, the waveform state selector switches to the rising edge. The edge address generator generates the rising edge address and passes it to the edge memory to output the waveform sample points, and the waveform generator generates the analogue waveform according to the sample points. When the phase value exceeds the rising edge phase value, the waveform state selector switches to the high-level and the edge address generator generates the high-level address. When the phase accumulator accumulates the phase corresponding to the falling edge, the waveform state selector switches to the falling edge, the

falling edge address generator starts to generate the falling edge sample point address, and the address selection module outputs the address. The generation process of the low-level is similar to that of the high-level. Where the state of the pulse waveform is judged by the waveform state selector on the basis of the phase value P to determine the specific state that the waveform is in. As shown in Fig. 5, the values of *P1*, *P2*, *P3*, and *P4* are calculated by (8) (9) (10) and (11) respectively, T_R is the rising time, T_F is the falling time, and T_W is the pulse width.

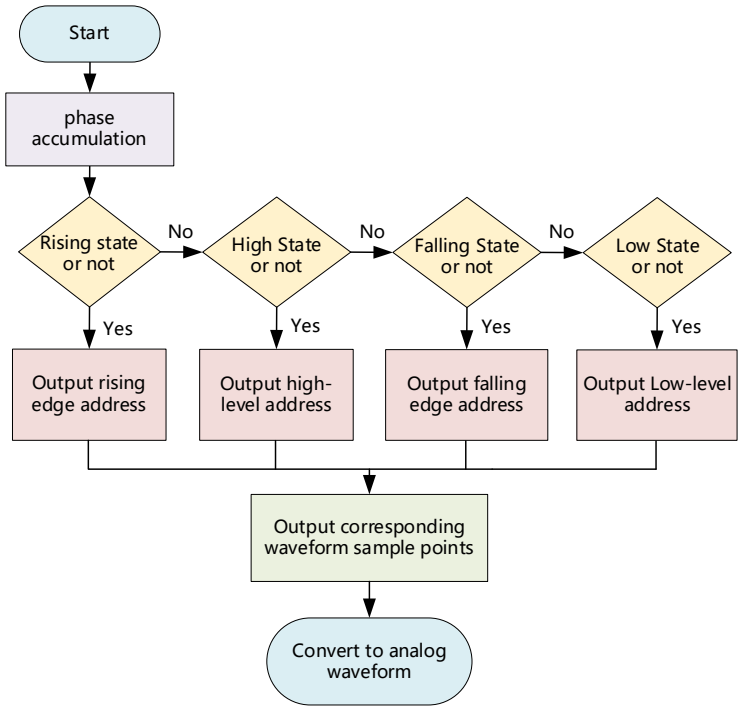

Fig. 4. Pulse waveform generation process.

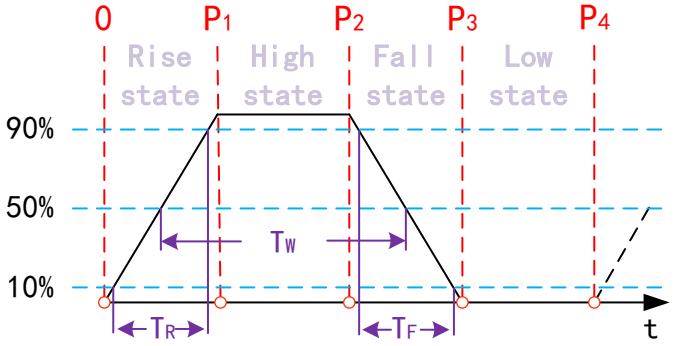

Fig. 5. Waveform state judgement.

$$P1 = \frac{T_R \times K}{0.8 \times T_S}. \tag{8}$$

$$P2 = \frac{(T_R + 1.6T_W - T_F) \times K}{1.6 \times T_S}. \tag{9}$$

$$P3 = \frac{(T_R + 1.6T_W + T_F) \times K}{1.6 \times T_S}. \tag{10}$$

$$P4 = 2^N - 1. \tag{11}$$

Due to the change of the waveform sampling storage content, the phase value provided by the phase accumulator cannot match with the new storage content, thus failing to generate the correct sample point value, and the method of directly calculating the waveform sampling amplitude value is too complicated. To solve this problem, an adaptive phase adjustment algorithm is proposed in this paper. The algorithm adjusts the initial phase of the next cycle by using the waveform phase overflow value of the previous cycle, and adjusts the edge position by combining the basic principle of resolution enhancement, so as to accurately output the waveform sample point value. To analyze the above example in Section 2.1, assuming that the sampling frequency f_S = 1 GHz, the pulse frequency f = 1/16.7 GHz, the pulse width T_W = 8 ns, the rising edge T_R, the falling edge T_F are both 3.2 ns, and the edge samples N_{total} = 40, for ease of analysis and to ensure frequency accuracy, the phase totalizer bit width N is set to 32 bits, and the frequency control word $K \approx 257183670$ is calculated from (8). The synthesis process of the feature-fitting pulse waveform is shown in Fig. 6.

$$K = \frac{f \times 2^N}{f_S}. \tag{12}$$

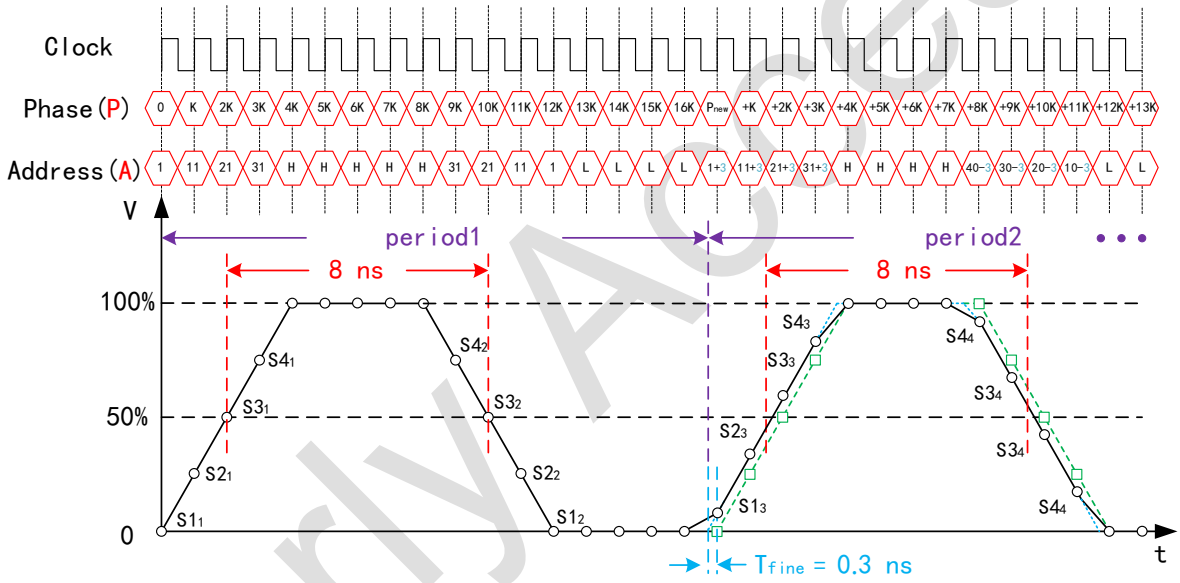

Fig. 6. Synthesis process of pulse waveform.

The accumulator accumulates after triggering on the falling edge of the sample clock, while the edge address generator changes the output. The edge address generator is read on the rising edge of the sample clock. If the initial phase offset of the waveform is 0°, the initial value of the phase accumulator is 0 and the frequency control word K is used as the accumulation step. In the 1st cycle, the rising edge left shift time T_{fine} is 0, the rising edge address generator address offset value is 0, according to (9), the address accumulation step D is 10. When the address generator accumulates 4 times, the rising edge ends, and at this time, the phase accumulator accumulates to 4K, and the waveform state selector judges that it enters the high-level state, so the address generator outputs the high-level address (H). When the phase accumulator accumulates to 9K, the waveform state selector judgement enters the falling edge state, and the waveform sample point is addressed by the address generator to the edge memory and output. The pulse width is 8 ns, and the starting position of the falling edge of cycle 1 is calculated to be 9 ns. The amplitude value of the sample point of the falling edge waveform changes from a large to a small value, corresponding sample point value $S4_2$ is equal to $S4_1$, and the address generator sends out the address in a gradual decrease in steps of 10. The address generator outputs the address 4 times and then the falling edge ends, at this time the phase accumulator

accumulates to 13*K*, the waveform state selector judgement enters the low-level output state, so the address generator outputs the low-level address (L). When the phase accumulator accumulates to the 18th sampling clock, the phase value overflows and the overflow value P_{new} = 17*K* - 2^N = 77155094, which enters the 2nd cycle. The value of P_{new} is automatically calculated by register overflow.

$$D = \frac{T_S}{T_{res}}. \tag{13}$$

The phase overflow value from cycle 1 to cycle 2, P_{new}, corresponds to a time of 0.3 ns. The waveform samples in cycle 2 are advanced by 0.3 ns compared to the green conventional waveform. This means that at the 18th sampling clock, the phase accumulator value is P_{new}, the rising edge waveform sample point in cycle 2 corresponds to an edge amplitude value of T_{fine} = 0.3 ns, and the address offset of the rising edge address generator address is offset by T_{fine}/T_S = 3. The formula for calculating T_{fine} is summarized in (10). Address AR_1 is calculated from (11) as 4 corresponding to sample point $S1_3$, address accumulation step is 10, address AR_2 is 14, and (12) summarizes the rising edge address calculation. Continue to output the address until the 4 waveform samples are output. At the 22nd sample clock, the phase accumulator has accumulated to P_{new} + 4*K* and the address generator outputs a high-level address (H). At the 26th sample clock, the phase accumulator value is P_{new} + 8*K* and the waveform segment enters the falling edge. The first waveform sample point on the falling edge is also advanced by 0.3 ns with an address offset of 3. The address of AF_1 (41 – 3) from (17) corresponds to the sample point value $S4_4$. The address is decremented in steps of 10 to generate the addresses of the four waveform sample points. At the 30th sample clock, the value of the phase accumulator is P_{new} + 10*K* and the address generator outputs a low address (*L*). This is repeated for subsequent cycle waveform samples.

$$T_{fine} = \frac{P_{new} \times T_S}{K}. \tag{14}$$

$$A_1 = 1 + \frac{T_{fine}}{T_{res}} = 1 + \frac{P_{new} \times T_S}{K \times T_{res}}. \tag{15}$$

$$AR_n = AR_1 + (n-1) \times D = 1 + \frac{\left[(n-1) \times K + P_{new}\right] \times T_S}{K \times T_{res}}. \tag{16}$$

$$AF_1 = NF_{total} + 1 - \frac{T_{fine}}{T_{res}} = NF_{total} + 1 - \frac{P_{new} \times T_S}{K \times T_{res}}. \tag{17}$$

$$AF_n = AF_1 - (n-1) \times D = NF_{total} + 1 - \frac{\left[(n-1) \times K + P_{new}\right] \times T_S}{K \times T_{res}}. \tag{18}$$

Through the above analysis, it is not difficult to find that to achieve the same rise time and fall time, only a set of edge timing sample points are needed to achieve the synthesis of the rising and falling edges. If different rise and fall times are to be realized, then two different sets of edge time samples need to be stored according to the edge adjustment principle.

3. Simulations

In this paper, MATLAB is used for simulation and analysis to verify the feasibility of the proposed method. To reflect the performance of timing resolution, a preliminary simulation is

conducted where the periods of the pulse waveforms are set to 16 ns, 16.1 ns, 16.2 ns, and 16.3 ns, respectively. The rise time and fall time are both set to 3.2 ns, and the pulse width is 8 ns. The simulation settings include a sampling period of 1 ns, amplitude normalization to 1, and a total of 40 sample points stored in the edge memory. The standard deviation of time jitter (including clock jitter and DAC jitter) is set to 10 ps; the standard deviation of amplitude jitter (referring to the fluctuation of DAC output amplitude) is set to 0.005; and the standard deviation of Gaussian white noise is also set to 0.005. The simulation results are shown in Fig. 7. By zooming in on the rising edge of the second cycle, it can be observed that the green rising edge is delayed by 0.2 ns, the yellow rising edge by 0.4 ns, and the pink rising edge by 0.6 ns compared to the initial blue rising edge.

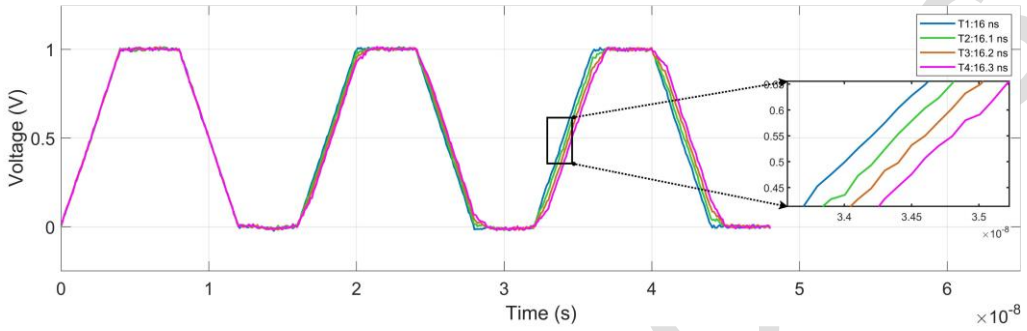

Fig. 7. Simulation results.

The four pulse signals were measured separately using the MATLAB built-in oscilloscope module and the results are shown in Fig. 8. It can be observed that the temporal resolution of the pulse period reaches up to 100 ps with other parameters remaining almost unchanged.

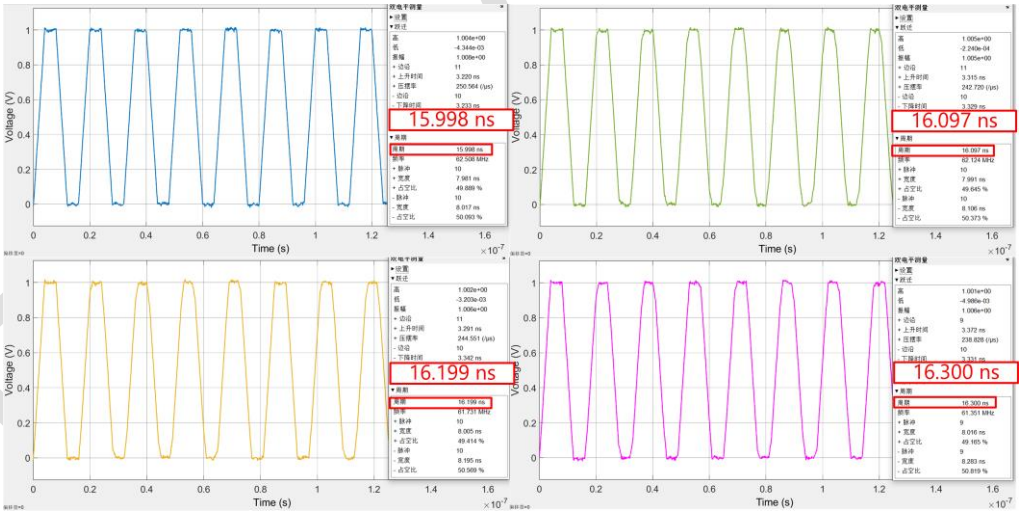

Fig. 8. Simulation oscilloscope results.

In further simulation analysis, the effects of time jitter, amplitude jitter, and Gaussian white noise on the pulse signal characteristics are investigated in detail. These factors correspond to clock jitter, DAC jitter, DAC output amplitude fluctuation, and background noise in the hardware system, respectively. Analyzing these factors helps to comprehensively evaluate the performance of the proposed method in complex environments and the variation in timing resolution. The simulation is configured with a pulse waveform period of 16.7 ns, rise and fall times of 3.2 ns, and a sampling period of 1 ns. Figure 9a illustrates the effect of time jitter on the pulse period, with the horizontal axis representing the standard deviation of time jitter.

Figure 9b shows the effect of amplitude jitter on the pulse period, with the horizontal axis representing the standard deviation of amplitude jitter. Figure 9c illustrates the effect of Gaussian white noise on the pulse period, with the horizontal axis representing the standard deviation of Gaussian white noise.

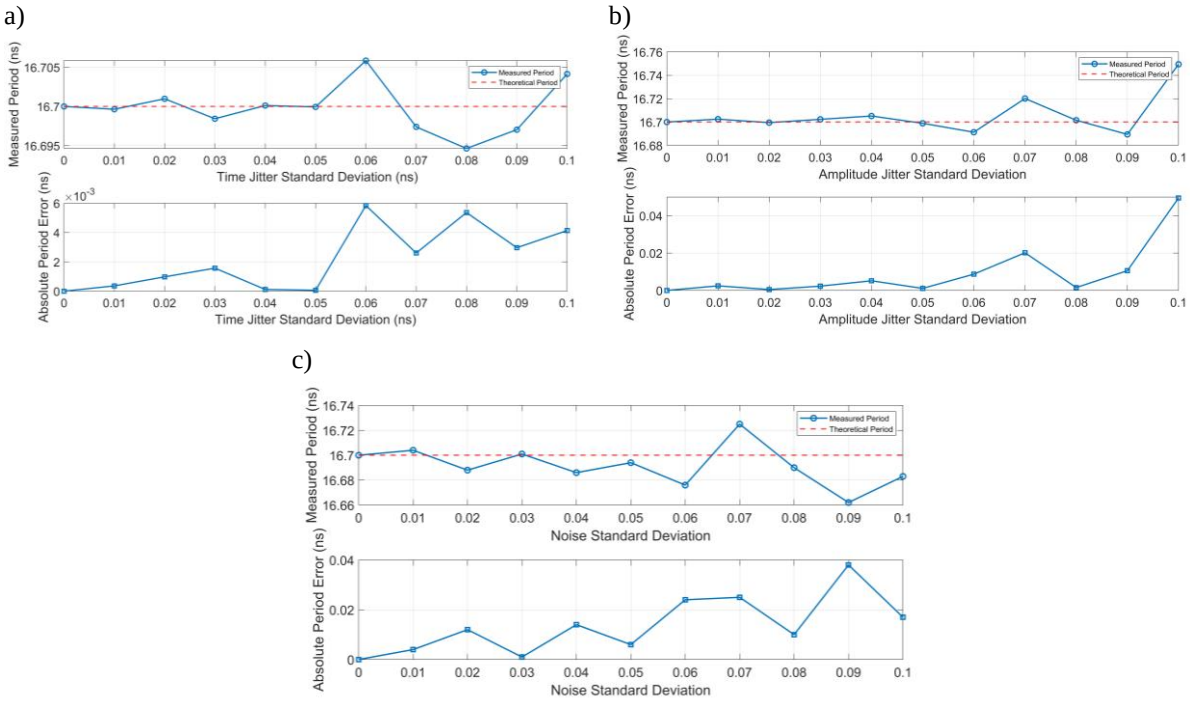

Fig. 9. Environmental and noise impact test. a) effect of time jitter. b) effect of amplitude jitter. c) effect of Gaussian white noise.

4. Testing and analysis

To verify the practical feasibility of the method, an experimental platform based on a Xilinx FPGA chip was built. The structure of the platform is shown in Fig. 10. The waveform synthesis module consists of the Xilinx FPGA development board and the DAC39J82EVM development board from Texas Instruments. And the core includes the Xilinx FPGA XCKU040 chip and the Texas Instruments DAC39J82 DAC. The DAC features a 16-bit vertical resolution and a maximum sampling rate of 2.8 GSPS, with the experimental setup configured for 1 GSPS. The output pulse waveform is observed using an oscilloscope with a bandwidth of 6 GHz and a maximum sampling rate of 25 GSPS.

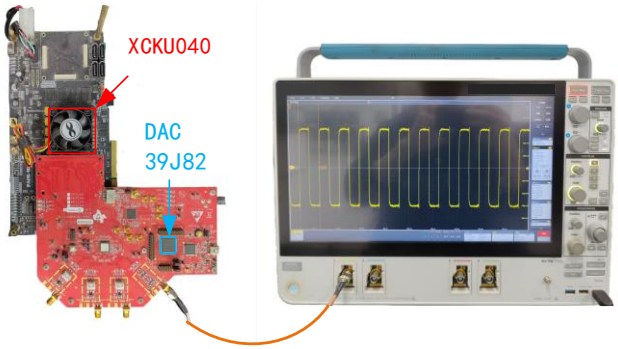

Fig. 10. Experimental test platform.

Table 2 shows the resources consumed by this scheme to achieve 100 ps timing resolution on FPGA and compares it with the other two sample point schemes and the DDS scheme (1 ns resolution). It can be seen that the real-time computation scheme is very expensive in terms of computational resources, consuming 2754 DSPs, LUTs and FFs. In contrast, this program consumes very little logic resources. After excluding other resource-consuming functions and designs, we focus our analysis on the logic resources consumed by the synthesis method. In contrast to the phase-amplitude mapping scheme, this scheme consumes some memory resources (*i.e.*, BRAM), but it consumes very few LUTs and triggers (FFs), especially computational resources, which are only two DSPs, whereas taking the computational scheme requires more DSPs. Regarding memory resources, the memory resources occupied by the edge samples are $40\times16 \text{ bits} = 640 \text{ bits}$ calculated by (6). Compared to the DDS scheme, which is limited to a time resolution of 1 ns, this scheme achieves a higher resolution with the same BRAM usage. This improvement is achieved by eliminating the storage space for high and low levels and increasing the storage of rising edge sample points. A DDS-based virtual sampling method is used to collect a larger number of samples [27], allowing the timing resolution to be increased to 100 ps, consuming memory resources of $10\times16\times16 \text{ bits} = 2560 \text{ bits}$. It can be seen that this scheme not only achieves higher resolution than the DDS, but also effectively saves memory resources.

Table 2. Consumption of FPGA resources

Design	Method	module	LUT	FF	BRAM	DSP
This work	feature-fitting DDS	entire design	5632	5936	51	2
		synthesis module	720	204	1	2
2024 [29]	phase-amplitude mapping	entire design	32456	31117	32	221
		synthesis module	6822	8655	0	192
2023 [30]	real-time computation	entire design	129698	136463	1064	2754
DDS (1 ns)	DDS	synthesis module	516	158	1	0

Starting with the verification of the synthesized pulse waveforms of the scheme, Fig. 11 shows the waveforms when the realization resolution of 100 ps, period is 16.7 ns, the pulse width is 8 ns, the rise time is 3.2 ns, and the fall time is 3.2 ns.

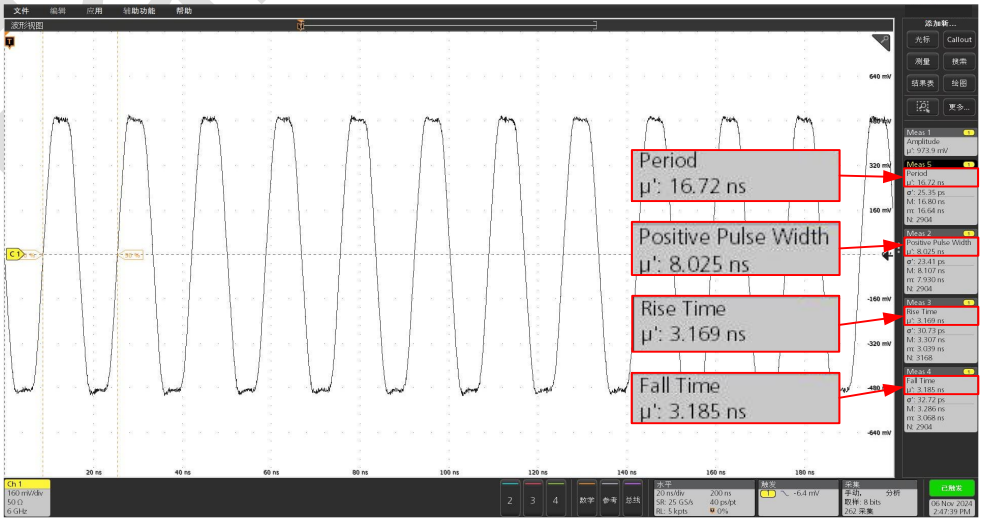

Fig. 11. Pulse waveform with a resolution of 100 ps, period of 16.7 ns, pulse width of 8 ns, rise time and fall time of 3.2 ns.

In order to verify the realization of the resolution, the resolution was initially set to 100 ps, and 12 pulse waveforms with different periods were generated. The periods ranged from 18.4 ns to 19.4 ns, incrementing in steps of 100 ps, as shown in Fig. 12a. Figure 12b shows the results of the test with a time resolution of 10 ps, where the period was incremented from 18.4 ns to 18.5 ns in steps of 10 ps. In order to measure the sample rate limitation, the impact on the resolution and waveform quality we conducted the following test, set the period to 100.3 ns, the rise time fall time is uniformly set to 8 ns, by adjusting the sampling period, to observe the rise time, the fall time and the period change. Figure 13 shows the variation between the rise time, fall time, and period during the sampling frequency 1000 MHz to 100 MHz.

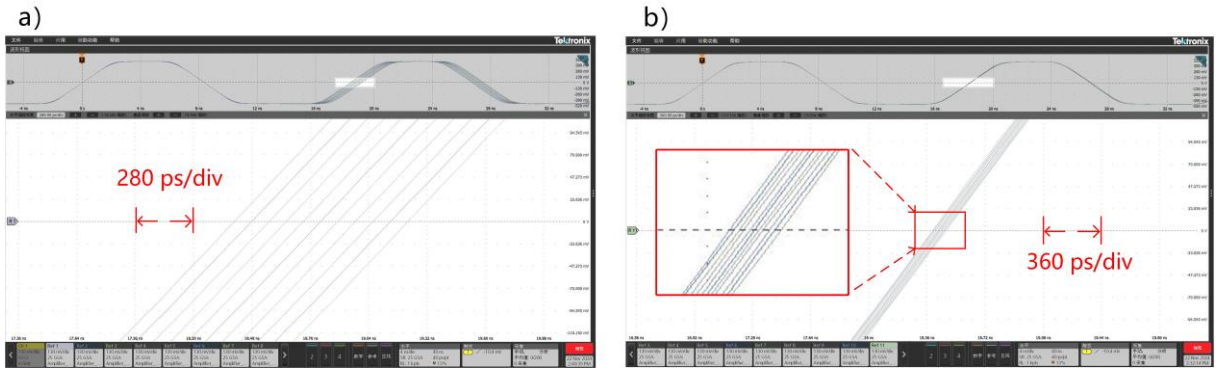

Fig. 12. Timing resolution test: a) pulse period with a 100 ps increment; b) pulse period with a 10 ps increment.

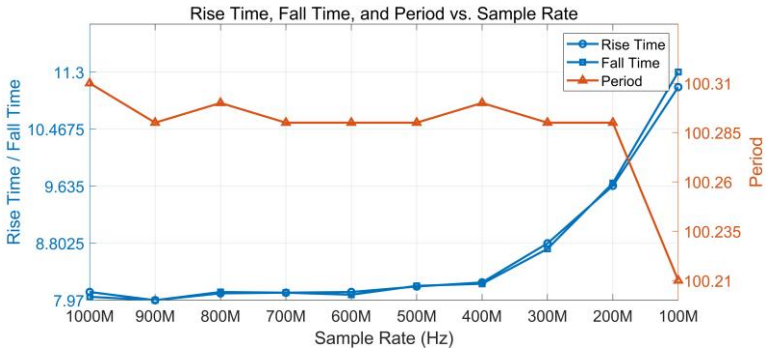

Fig. 13. Effect of Sampling Period on Waveform Parameters: Rise Time, Fall Time, and Pulse Period.

Modify the edge memory sampling points to verify the implementation of different edge times, uniformly set the period to 50 ns and the pulse width to 25 ns, and sequentially test the rising edge to 10 ns, the falling edge to 3.2 ns, and the rising edge to 3.2 ns, and the falling edge to 8 ns. The experimental results are shown in Fig. 14.

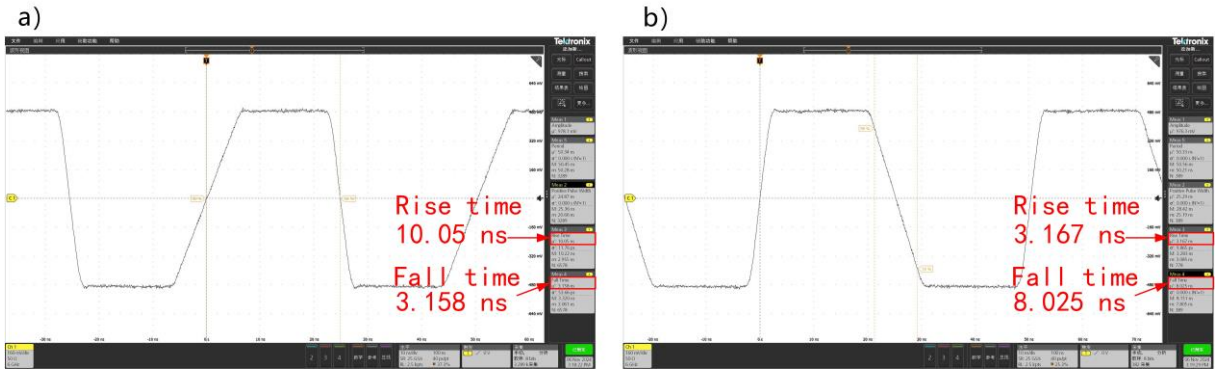

Fig. 14. Pulse edge time adjustment test a) The rise time is 10.05 ns the fall time is 3.158 ns. b) The rise time is 3.167 ns the fall time is 8.025 ns.

This design also enables amplitude control by proportionally adjusting the output waveform sample values. Figure 15 shows pulse waveforms incrementing by 100 mV, with peak-to-peak values ranging from 800 mV to 1.6 V.

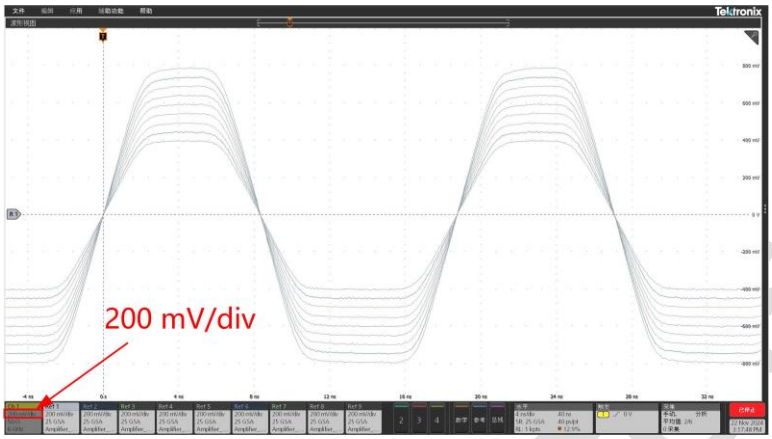

Fig. 15. Pulse peak-to-peak values in 100 mV increment.

To evaluate the jitter performance of the proposed design, jitter tests were conducted for both this scheme and a normal DDS. The jitter of the scheme at 1 ns and 100 ps resolution was tested to compare with the jitter of a 1 ns resolution plain DDS. The test counted about 50,000 samples, and the results are shown in Fig. 16. The experimental results show that the root-mean-square (RMS) of the *time-interval error* (TIE) of the scheme is 10.04 ps at 1 ns resolution and 10.04 ps at 100 ps resolution which is comparable to that of the normal 1 ns resolution DDS jitter of 10.26 ps. The very small change in jitter due to the change in resolution shows that the jitter of the proposed scheme is almost independent of the resolution, and the jitter mainly comes from the clock jitter and DAC jitter, which is consistent with that of normal DDS. Theoretically, the scheme only improves the way of storing and finding the sample points, while the way of outputting the sample points remains unchanged, so the jitter performance remains unchanged, as expected.

Table 3 compares the key parameters of this design with several FPGA-based pulse generators, including resolution, jitter performance, and support for edge adjustment and amplitude adjustment. This design has been experimentally verified for 100 ps and 10 ps timing resolutions, but its timing resolution is not limited to these values. Higher timing resolutions can be achieved through finer amplitude subdivisions of the edge time. In terms of resolution, this design is on par with or exceeds most DDS-based improvement schemes. Furthermore, unlike these methods, this design leverages feature storage to optimize the storage mechanism. It significantly reduces storage capacity requirements by storing only the feature sample points of pulse edges. For jitter performance, the design achieves a root-mean-square jitter of 10.04 ps. Since jitter primarily originates from the clock and DAC, employing a more stable clock source and DAC could further enhance performance. When compared to the 1.5625 ps resolution scheme in [31], which is based on Gigabit Transceiver (GT) architecture and relies on a high-performance clock, the design demonstrates competitive jitter performance. While this design is capable of achieving resolutions of 10 ps and, theoretically, even 1 ps or higher, its jitter performance does not improve with increased resolution. Additionally, it is fundamentally a binary pulse generator, which, despite being capable of high resolution, lacks functionalities such as edge time adjustment and amplitude adjustment.

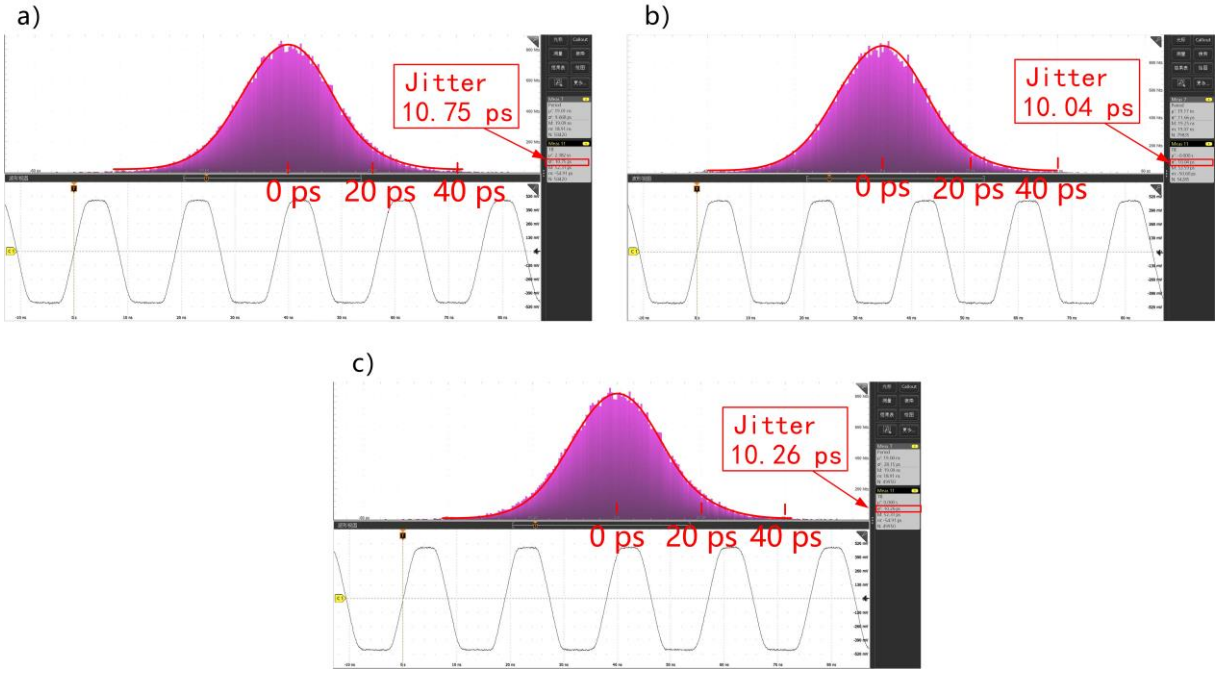

Fig. 16. Jitter test: a) of this scheme at 1 ns resolution, b) of this scheme at 100 ps resolution, c) normal DDS jitter at 1 ns resolution.

Table 3. Comparison with some other pulse generator.

Design	Device	Method	Resolution	Jitter (RMS)	Adjustable edge time	Adjustable amplitude
This work	Xilinx UltraScale+	feature-fitting DDS	100 ps, 10 ps[a]	10.04 ps	Y	Y
2024 [31]	Xilinx UltraScale+	high precision mode (A) based on GT	1.5625 ps	<1.5 ps	N	N
2024 [29]	Xilinx UltraScale+	phase-amplitude mapping	100 ps	N/A	Y	Y
2022 [27]	Xilinx UltraScale+	virtual sampling DDS	100 ps	24.31 ps (50 MHz)	Y	Y
2021 [24]	Altera Cyclone IV	re-configurable DDS	<10 ps	<30 ps	Y	Y
	Xilinx UltraScale+	DDS	1 ns	10.26 ps	Y	Y

[a] This value is related to the waveform sample acquisition settings.

5. Conclusions

In this paper, a pulse waveform synthesis method with feature-fitting is proposed. The adjustment principle, synthesis process, simulation verification, and hardware verification of the method are described in detail. The method achieves waveform synthesis by storing feature sample points, fitting the entire pulse waveform with edge sample points as features, and using DDS as a carrier. Since only the edge samples are stored, high timing resolution can be achieved with low memory consumption. On the other hand, the waveform samples are stored directly in memory, and the adaptive phase adjustment algorithm is used to find the address that realizes the accurate output of the samples without calculating the derived waveform samples, saving a lot of computational resources. Through our experiments, we successfully achieved timing resolutions of 100 ps and 10 ps, verifying the practicality and performance of this method.

Notably, this design is not limited to the aforementioned resolutions; higher resolutions can be obtained by further subdividing the amplitude differences between adjacent samples. In addition, the experiments confirm the flexibility of the design in adjusting both edge time and amplitude. This adaptability allows for greater demand in pulse waveform synthesis. The jitter performance of the design was also assessed, with the experimental results showing an RMS TIE of 10.04 ps, indicating the robustness of the system in maintaining high-quality signal integrity. This method not only provides an efficient and practical solution for generating high-precision pulse signals, but also offers valuable insights into the optimization of digital waveform synthesis technology, especially for applications requiring fine control over timing and amplitude.

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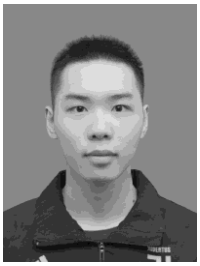
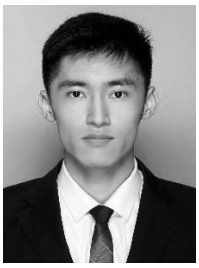


Yujie Deng was born in 2001. He is currently pursuing an academic master's degree in Instrumentation Science and Technology at University of Electronic Science and Technology of China, Chengdu, China. His research interests include pulse waveform synthesis and arbitrary waveform generator and pulse waveform generating technology and so on.

Zaiming Fu was born in Sichuan province, P.R.China, in 1977. He received Master's degree and PhD both from University of Electronic Science and Technology o*f Chi*na (UESTC), P.R.China in 2004 and 2010 respectively. Now he is a professor in school of automation engineering, UESTC. His research data generator and pulse generator, measurement and instrument, signal processing and so on.



Hanglin Liu received the B.S. and M.S. degrees in instrumentation engineering, in 2015 and 2018, respectively from the University of Electronic Science and Technology of China, (UESTC), Chengdu, China, respectively, and the Ph.D. degree in Instrumentation Science and Technology in 2023. His main research interest is automatic digital testing technology and Systems.

Dexuan Kong was born in 1997. He is currently working toward the Ph.D. degree in instrument science and technology with the University of Electronic Science and Technology of China, Chengdu, China. His research interests include instrument science and technology, automatic testing and system integration technology, arbitrary and pulse waveform generating technology and so on.

Xin Ai was born in 2001. He is currently working toward the Ph.D. degree in Instrumentation Science and Technology at University of Electronic Science and Technology of China, Chengdu, China. His research interests include pulse waveform synthesis and arbitrary waveform generator and pulse waveform generating technology and so on.